A density staggered cantilever for micron length gravity probing

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Abstract

A density staggered cantilever was developed to measure the micron length gravity between itself and an optically levitated microsphere in high vacuum. The cantilever, has two main density contrasted materials gold(19.3g/cm3) and silicon(2.33g/cm3), where each of the material is finger-shaped and stagger placed next to each other, constitute an integral finger array on the device layer of SOI wafer. The scallop of the DRIE defined fingers was optimized to be less than 50nm to reduce the surface variation between the cantilever and levitated microsphere. The end of each fingers were covered with 2-10um silicon and gold to shield the undesired charged particles. The back side of SOI wafer were defined with DRIE to release the cantilever. The Cantilever will be placed microns away from the microsphere and mechanically move back and forth to interact with the microsphere. This paper introduces the design, manufacturing of the density staggered cantilever for micron length gravity.

Introduction

Theories that attempt to unify gravity with the Standard Model or to explain the nature of dark energy suggest that gravity may deviate from the Newtonian form $1/r^2$ at micron length scales. Giorgio Gratta's group in Stanford University uses mesoscopic optomechanical systems to measure sub-attonewton forces at micron length scales to test these theories. Current work uses optically levitated microspheres to measure gravitational interactions between masses separated by less than 20 microns. Optically levitated microspheres provide a powerful probe for short-range forces because they can be precisely controlled with optics and do not need to be mechanically coupled to the surrounding environment. Recently, the group have used optically levitated microspheres to search for millicharged particles bound in the bulk of the microspheres.

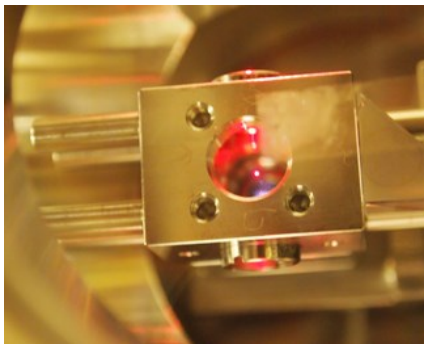

Figure1. Image of an optically levitated microsphere in vacuum

Design of the density staggered cantilever in micro gravity probing system

The amorphous silica microsphere with radius r=2.5um and mass m=0.13ng is levitated in a single-beam, upward-propagating 1064nm laser trap. The position of the microsphere is measured by focusing secondary 650nm Gaussian laser beams on the microsphere and imaging the pattern of scattered light onto a position-sensitive photodiode. Differential current is produced by the photodiode as a linear function of the position of microsphere [1,2].

The density staggered cantilever with dimensions of 525um ×500um×10um is going to be placed microns away from the microsphere. The tip end of the cantilever is restricted to have a roughness <50nm. The gold and silicon fingers are staggered with individual width of 25um. The cantilever will be driven to move back and force to interact with microsphere for the micron length gravity measurement.

Fabrication of density staggered cantilever

1. Material selection

In order to achieve a large contrast in density on the cantilever, different groups of material candidates were investigated. Gold(19.3g/cm^3) and silicon(2.33g/cm^3) were chosen because they are semiconductor process compatible materials as well as have a ratio of mass density of 8.28.

The SOI wafer consists of a device layer, buried oxide and bulk silicon. To precisely interact with laser levitated sphere and clear the Gaussian beam waist of the laser [2], the device layer needs to be sufficiently thin. But to maintain the mechanical stability of the cantilever, the device layer should be rigid enough to support the standalone outreaching part, therefore a 10um device layer was chosen. For the buried oxide, it should not only maintain the integrity during the front and back side deep silicon etch, but also introduce the stress as low as possible, so the buried oxide was chosen to be 0.5um thick. The thickness of bulk silicon depends on the feasibility of installing the component in the mesoscopic system which was chosen to be 350um.

2. Patterning

The wafer is 4-inch (100) N-type prime wafer, rinsed in 5:1:1 H_2O:H_2O_2:NH_4OH, 50:1 HF and 5:1:1 H_2O:H_2O_2:NH_4OH to remove residual particles, native oxide and polymer. Then baked in nitrogen oven at 150C for 15mins to remove the H_2O vapor on the surface. To photo define the shape of cantilever on the device layer, the main factors are selectivity between mask and silicon, sidewall roughness, no/low grassing at the bottom of deep trench, and the etching chamber needs to be reasonably clean to grow dioxide film.

The first test run was on the ICP etcher. The mask was the combination of photoresist and CCP-CVD deposited silicon dioxide with 7um and 2um. The test run indicated 8:1 silicon to oxide etch ratio, and 1:1:8 photoresist and oxide etch ratio. However, deteriorated grassing effect was observed at the bottom of the via. A descum process was added after the

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lithography, but the grassing problem still remained as in Figure2.

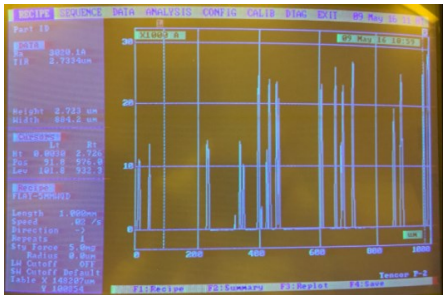


Figure2. Grassing at the trench bottom after ICP etching

The second run was on the deep reactive ion etcher (DRIE). DRIE has high selectivity between photoresist and silicon, ~110:1, only 1.6um AZ3612 photoresist was coated to achieve good patterning. But the main challenge for DRIE was the scallop on the sidewall due to the nature of BOSCH process. BOSCH process mainly consists of two important steps: etching and passivating. Passivation cycle uses C4F8 to deposit polymer on the bottom and sidewall of the trench, while etching cycle uses SF6 to etch the deposited polymer and silicon beneath it. To control the size and depth of the scallop, we divided the etching step into two individual steps, Etch A to remove the deposited polymer with 150sccm SF6 and 1500W ICP power, then Etch B starts to etch silicon device layer with 50sccm SF6 and 1300 ICP power. The loop left the sidewall with small sized scallops, but was able to etch the silicon vertically. The sidewall profile is shown in Figure3, where the scallop length was ~185nm, and depth was ~46nm.

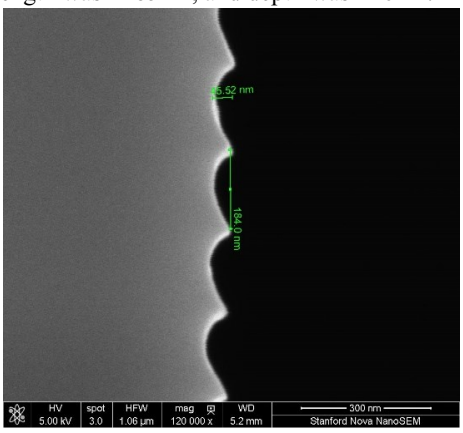
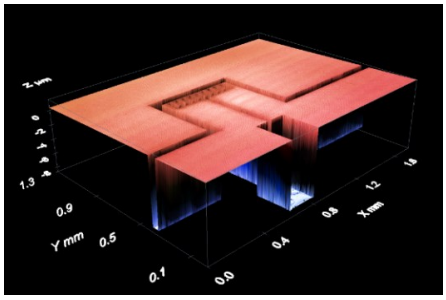
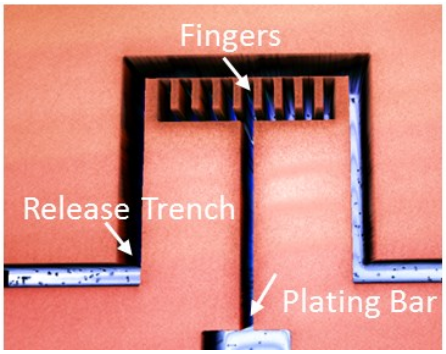


Figure3. Sidewall profile with <50um scallop on the cantilever tip

Bottom notch was minimized by precise control of the cycle numbers and the power distribution across the wafer. 3D optical profiler obtained the non-invasive assessment of the micro geometry of the technical surface of the cantilever, see Figure4.



(a)



(b)

Figure4. (a) Cantilever 3D profile with 45 degree view (b) Cantilever 3D profile with 90 degree view

After the deep trench etch, Piranha solution with 9:1 H_2SO_4:H_2O_2 at 120C was applied to remove the BOSCH produced polymer on the trench sidewall. The minimum width of the trench tip was 2um.

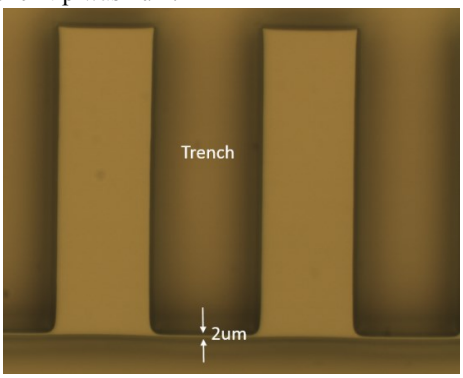


Figure5. Minimum finger tip of the cantilever

3. Liner deposition

SiO_2 insulator was used to cover 10um trench on the device layer. The step coverage was ~60%, 500nm SiO2 across the wafer was grown, and the thickness at the bottom of via is ~300nm. To be noticed that there were pin hole observed at the sidewall, since the wafer is thoroughly cleaned before sticking into the CVD chamber, it presumably the chamber was not sufficiently clean for the deposition. However, as the fabrication adopted the bottom-up via-filling technique, the pinholes on the trench sidewall was trivia.

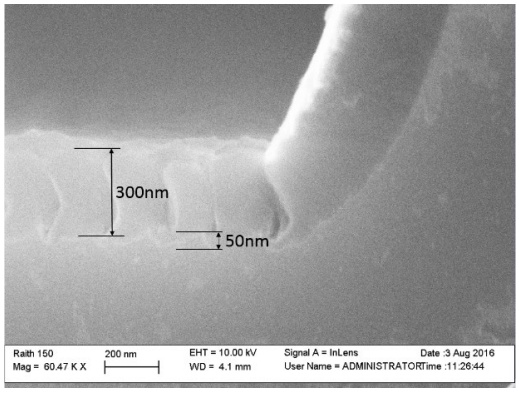


Figure6. Oxide deposition in the trench

Highly directive evaporation system was then used for seed layer deposition. The reason to choose evaporation instead of sputtering is evaporation and electroplating thereafter is able to create weak bond between metal and insulator so it is possible to singulate the cantilever from the wafer without metal in the outline trench attached. The seed layer consists of 20nm Titanium and 50nm Gold, and the seed layer was deposited on the horizontal surface only, i.e. the bottom of the trenches are disconnected from the seed layer on the top surface of the wafer.

4. Metal filling

Chemical mechanical polishing (CMP) was used to remove the Ti/Au from the top surface. We chose Al_2O_3 slurry with pH=3-5, and low contact pressure for both polishing and retainer ring. The removal rate is approximately 11nm/min. Afterwards, the Titanium is removed by 10:1 HF. One thing to be noticed is HF also attacks the exposed buried oxide, but etch rate is 23nm/min, while Titanium is removed much faster at 1100nm/min. After etching for a few seconds, the wafer is DI water rinsed and dried for electroplating.

A dedicated electroplating jig for cantilever electroplating was designed. The conductive rod connects the current source to the meshed anode through four tightly pinched shims. The anode was installed on a Teflon backing plate. On the backing plate, several large sized trenches were fabricated to ensure the mobility of the electrolyte across the structure. Four pogo pins were inserted through the Teflon backing plate with no shorting to the anode, and made good contact with the cathode, i.e. the wafer to be electroplated. The shortcoming of the structure was the unwanted area to be plated and lead to the difficulties of calculating the plating area. To solve this problem, the PTFE shrinkable tubes were mounted on the pogo pins and connected wires to limit the extra plating area. Since the spring in the pogo pins ensures sufficient pressure to the plating pad on the wafer, in the process of plating, the current density changes only with the metal thickness in the trench.

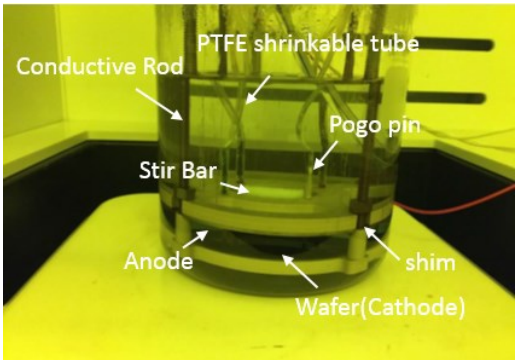


Figure6. Customized plating jig

In order to control the bottom-up plating process, we chose pulse reverse current(PRC) plating technique over direct current (DC) plating because of [3]:

(1) PRC continuously raises limiting current density significantly by replenishing metal ions during the whole process time of plating
(2) Deposition composition, structure, porosity and hydrogen content can be obtained with PRC
(3) PRC reduces additive requirement significantly while enhances bath stability and efficiency
(4) PRC eliminates thickness build up at high current density areas during current reversal and improves step coverage.

Duty cycle corresponds to the percentage of total time of a cycle,

$$\text{duty cycle} = \frac{T_{ON}}{T_{ON}+T_{OFF}} \quad (1)$$

Current density is chosen to be 0.3ASD, the average current can be calculated as:

$$\bar{I_A} = \frac{I_C T_C - I_{AA} I_{AA}}{T_{AA}+T_C} \quad (2)$$

Where I_C is cathode current density, I_{AA} is anode current density, T_{AA} is reverse time, and T_C is forward time. The anode area is 0.65dm^2, cathode area is 0.06dm^2, cycle length is 5sec, duty cycle is 40%. The calculated I_C is -132mA, and I_{AA} is 130mA. A dedicated electroplating current source was used as shown in Figure7 along with the plating waveform.

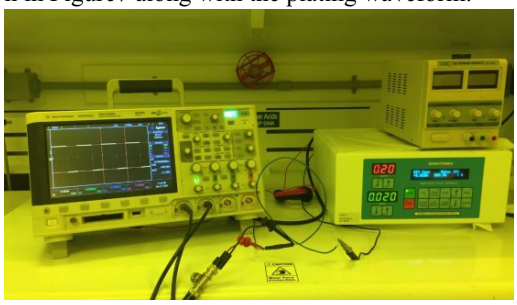


Figure7. PRC electroplating current source and waveform

We tried cyanide and sulfuric gold electrolytes, while cyanide plating introduces larger grain size with pin holes.

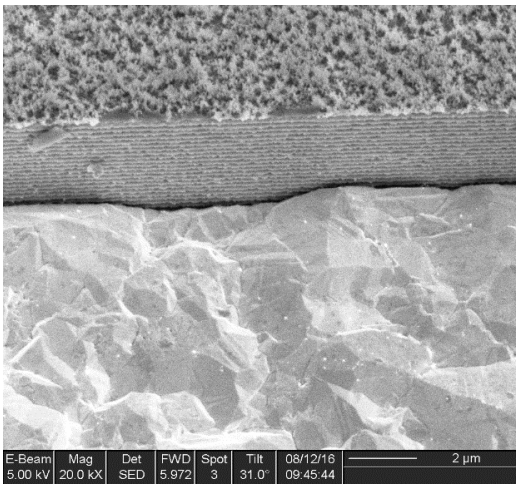


Figure8. Gold grains grown in cyanide electrolyte

The preferable sulfuric solution with pH=8.5 is used to electroplating the trenches with equivalent 0.3ASD for ~1.5hrs plating. Additive is added and stirred when plating rate has significantly dropped. The morphology of the plated gold is much smoother for sulfuric solution, see Figure9.

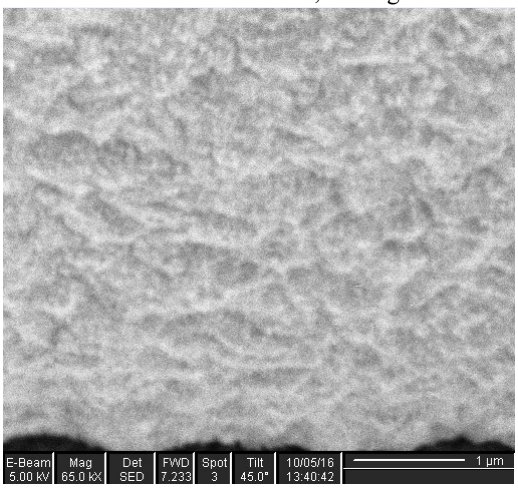


Figure9. Gold grains grown in sulfuric electrolyte

The wafer was chemical mechanical polished before plating, although we had sonicated the wafer before plating, there was still a chance the electrolytes gets polluted, a vacuum filter system was applied for filter >0.2um particles to purify the electrolytes.

5. Planarization

The wafer was planarized with CMP, unlike polishing the seed layer, the mechanical strength of plated gold allows higher pressure of polisher and retainer ring, the spin rate was also increased to remove gold at reasonable fast speed, see Figure9.

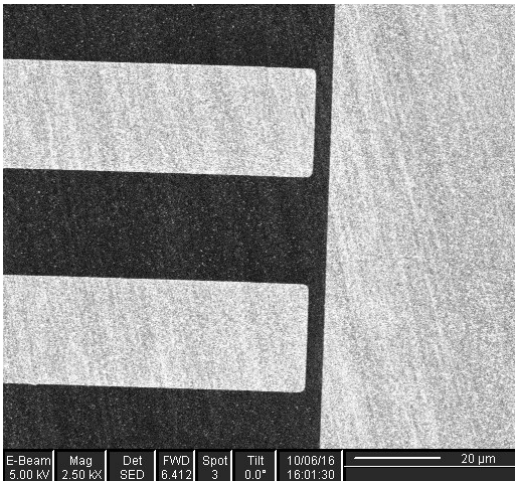


Figure9. Planarized cantilever

6. Backside Patterning

A deep trench etching from the bulk silicon to buried oxide layer was adopted. The bulk silicon is 350um thick, photoresist as the only mask is expected to lead to unacceptable sidewall taper. According to the SiO_2-Si selectivity, 2.2um SiO_2 was deposited on the backside of the wafer. On the SiO_2, 1.6um AZ3612 was coated, exposed and developed. After descum process, we used RIE to etch the hard mask with CF_4, CHF_3 with helium cooling. The power was 500W.

The wafer was transferred to DRIE equipment for high selective silicon etch, the endpoint was constantly monitored to find the moment the buried oxide was reached. As seen from Figure10, the backside trenches uniformly reached the buried oxide layer without causing wafer warpage or damaging any cantilevers.

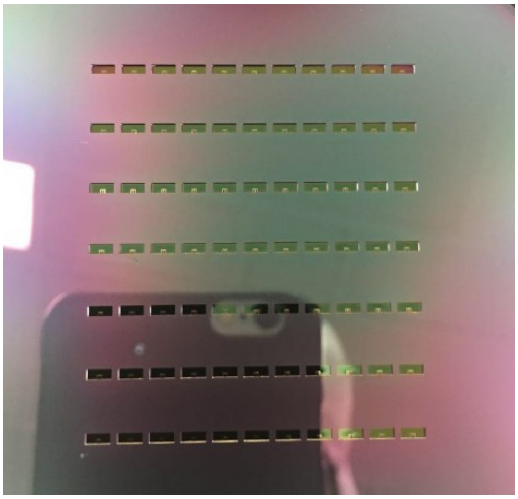


Figure10. Buried oxide exposed after backside DRIE

7. Cantilever release

Buried oxide layer was etched by 1:10 HF. The area of the cantilever sitting on the oxide was released. However, the cantilever was too fragile to survive the mechanical impact, which would cause problems during singulating the devices. We used syringe to inject the viscous AZ4620 into the backside trench and carefully remove the photoresist protrude the surface.

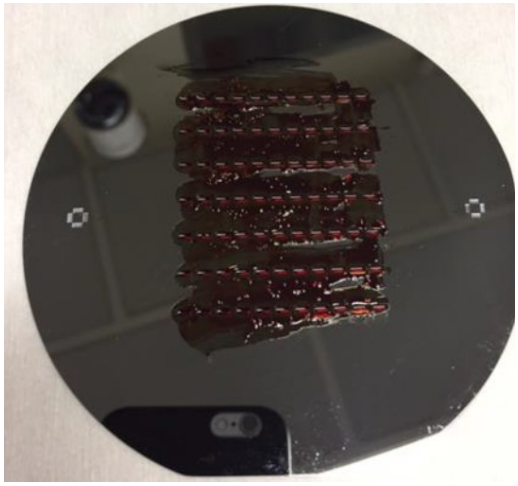


Figure11. Manually strengthen the cantilever with viscous liquid before removing the photoresist on the surface

After curing the photoresist, the wafer was attached to the adhesive film and diced. Due to the loosely bond between the metal on the release trench and the sidewall, most of the devices were properly separated from the wafer. The other cantilevers were capable of shake off the metal on the release trench after carefully sonicated with low power in DI water.

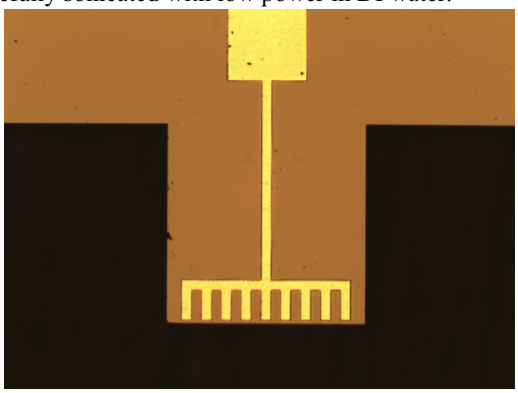


Figure12. Singulated cantilever on optical microscope

Further development

The sigulation of the cantilever, including mechanical strengthen with polymer and wafer dicing, was elaborating. We developed a self singulating process to release the structure without dicing or any of the mechanical strengthen process. The topside cantilever outline which defined firstly is slightly larger than the bottom side outline, therefore, after back side DRIE and buried oxide removal, the hanging part at the handle of the device can be easily broken off from the wafer.

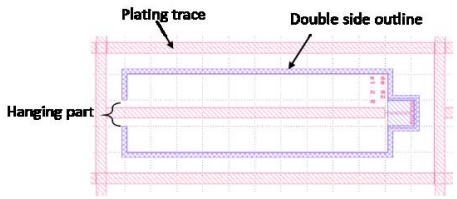


Figure13. Self sigulation design

The singulated density staggered cantilever is shown in Figure12.

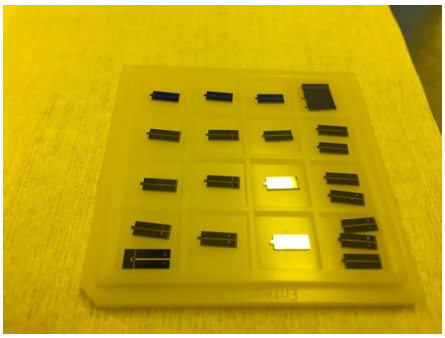
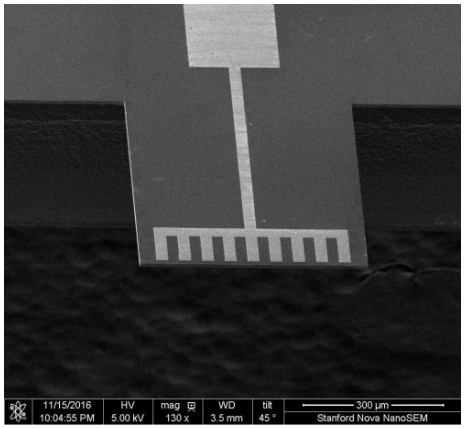


Figure14. Singulated cantilevers

SEM of the density staggered cantilever

The density staggered cantilever is fabricated. The 10um thick cantilever sticking out from the bulk silicon with the area of 525um ×500um×10um.



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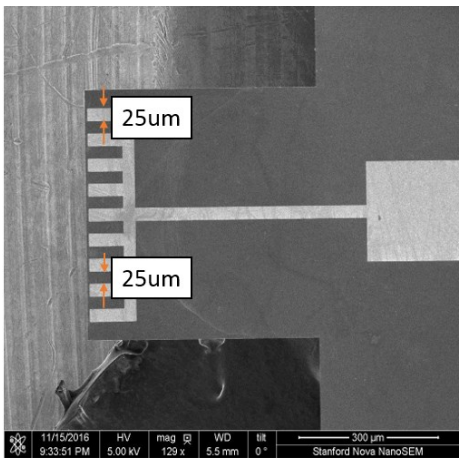

(b)

Figure15. SEM of the density staggered cantilever

Conclusion

A density staggered cantilever is developed with gold and silicon staggered in parallel. Design and fabrication of the cantilever for micron length gravity is discussed in detail. Further work involves mounting the structure in the testing system, and developing new structure with no mechanical vibration system.

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